

Implantation-Free 4H-SiC Bipolar Junction Transistors with Double Base Epi-layers

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Abstract— This paper reports the first 4H-SiC power bipolar junction transistor (BJT) which is completely free of ion implantation and hence is free of the implantation-induced crystal damages and high-temperature activation annealing-induced surface roughness. The BJT is designed to have double epitaxial p-type base layers with the top layer more heavily doped for direct Ohmic contact formation while at the same time supporting a robust single-step junction termination extension without the need of ion implantation. The double layers create a built-in electric field in the base region which helps to speed up injected electrons across the base and leads to an improve BJT current gain. Based on this novel design and implantation-free process, a 4H-SiC BJT has been fabricated to reach an open base collector-to-emitter blocking voltage of over 1300 V with a current gain up to 31, using a drift layer of 11.5 μm , lightly-doped to $8.5 \times 10^{15} \text{ cm}^{-3}$.

Index Terms—Silicon carbide, bipolar junction transistors (BJTs), power transistors

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I. INTRODUCTION

4H-SiC bipolar junction transistor (BJT) is an important switching device for high power and high temperature applications. It is an intrinsically normally-off device, does not have gate oxide problems as in SiC MOSFET and IGBT, and conducts high current with a low forward voltage drop. For 4H-SiC BJTs, high current gain is desirable in practical applications for simple control circuit design and better energy efficiency. Many studies have been reported to further increase the current gain of 4H-SiC BJTs by optimizing the emitter/base geometry [1], surface passivation [2], ion implantation [3], as well as employing continuous growth of the base and emitter epi-layers in the same reactor [1,4-6]. In the fabrication of 4H-SiC BJTs, the base Ohmic contact is usually formed on a heavily implanted p+ region. The p+ implantation also requires an activation annealing at high temperature, normally over 1500°C. This base ion implantation process introduces crystalline damages both inside the base region and on the surface of SiC, resulting in an increased base recombination current and lowering the current gain. Our earlier experimental study showed that lower base implantation energy and dose resulted in higher current gain 4H-SiC BJTs [2]. We also reported that BJTs with unintentionally graded base doping tend to have higher current gains [7] because the built-in electric field resulting from the graded base epi-layer helps the injected electrons from the emitter to move quickly through the base, reducing the base recombination. This paper reports our first experimental effort with BJTs intentionally designed with a non-uniform base doping that will have the desired built-in electric field in the base region while making it possible to form p-type Ohmic contact to the base without ion implantation.

II. DEVICE DESIGN AND FABRICATION

Fig. 1 shows a cross-sectional view of the fabricated 4H-SiC BJTs. The wafer is purchased commercially per our design. The base and emitter epi-layers are grown in separate reactors, similar to those BJTs reported before [8-10]. The emitter n^+ epi-layer is 0.3 μm thick, and is doped to $2.0 \times 10^{19} \text{ cm}^{-3}$. The base epi-layer consists of a 0.40 μm , $1.0 \times 10^{17} \text{ cm}^{-3}$ lightly doped epi-layer capped by a 0.15 μm , $4.6 \times 10^{18} \text{ cm}^{-3}$ heavily doped top epi-layer. The drift layer is 11.5 μm thick and lightly-doped to $8.5 \times 10^{15} \text{ cm}^{-3}$ grown on n-type buffer layer of 0.5 μm , doped to $1.0 \times 10^{18} \text{ cm}^{-3}$ on a heavily doped n-type 4H-SiC substrate.

The fabrication process starts with a dry etching of the emitter fingers by inductively coupled plasma (ICP) in a gas mixture of freon and oxygen at an etching rate of 70-80 nm/min. The p-type epi-layer was exposed in the base trench and the junction termination extension (JTE) region. A single step JTE with a width of 160 μm , based on the remaining 0.48 μm p-type base epi-layer, is formed for the edge termination. The isolation between each device is created by a mesa etching of $\sim 1.6 \mu\text{m}$ into the drift layer. The sample is oxidized by a wet thermal oxidation for 2 hours at 1100°C followed by a 1-hour Ar annealing at 1100°C and a re-annealed in wet-oxygen for 3 hours at 950°C. After the thermal oxidation, 380 nm SiO_2 and 250 nm Si_3N_4 are deposited by PECVD to seal the thermal passivation layer. Base Ohmic contact is directly formed on the p-type epi-layer, with a designed spacing between the base contact region and the emitter mesa edge (BE-spacing) of 6 μm . Base contact metals are based on sputtered AlTi and Ni while emitter and collector Ohmic contacts are both based on sputtered Ni. The Ohmic

contact annealing is carried out at 1000°C for 5 minutes in Argon forming gas (5% H₂ in Ar) by using a rapid thermal processing (RTP) system. After Ohmic contact formation, a thick layer of AlTi/Al/AlTi is sputtered on the base and emitter fingers to improve the voltage and current distribution along the fingers. Then, SiO₂ and Si₃N₄ multi-layers are deposited by PECVD as the insulator between the overlay metals. The base and emitter contact windows are opened by ICP. Sputtered Ti / Au are used to form the base and emitter bonding pads as well as the collector overlay metal on the substrate.

Fig. 2 shows a top-view photo of a fabricated small area 4H-SiC BJT. It has an eccentric circular geometry. The device outer diameter is 600 μm . The emitter mesa is 18 μm wide, and forms an emitter mesa ring in the inner circle. The base contact region also forms a ring outside of the emitter mesa ring with a width of 10 μm . The emitter bonding pad is inside the circle formed by the emitter mesa with dielectrics insulated from the p-type 4H-SiC surface. The base bonding pad is formed at one side of the emitter, sitting directly on dielectrics.

III. EXPERIMENTAL RESULTS AND DISCUSSIONS

Measured from the on-chip TLM (transmission line model) structure, the emitter n-type specific contact resistance and n⁺ emitter layer sheet resistance are $1.0 \times 10^{-5} \Omega \cdot \text{cm}^2$ and 228 Ω , respectively, while the p-type specific contact resistance and p-base sheet resistance are $6.3 \times 10^{-3} \Omega \cdot \text{cm}^2$ and 87 k Ω , respectively, as shown in Fig. 3. The base specific contact resistance is close to the value obtained from the implanted samples, showing that the doping concentration of $4.6 \times 10^{18} \text{ cm}^{-3}$ can provide a reasonable p-type

Ohmic contact. The sheet resistance of the p-type base layer is larger by a factor of 2, compared to our previously implanted BJT samples, most likely due to the smaller thickness of the base layer and the lower doping of the remaining base of the BJT design.

Fig. 4 shows the common emitter I-V characteristics of a fabricated circular small area 4H-SiC BJT as shown in Fig. 3. It conducts 93.5 mA collector current when the base current is 3.0 mA, corresponding to a very good DC current gain of 31.2. The open emitter blocking voltage (V_{CBO}) is up to 1810 V, and its open base blocking voltage (V_{CEO}) is 1336 V. Fig. 5 shows the common emitter I-V characteristics of a large area 4H-SiC BJT fabricated on the same double base epi-layer wafer. It has a footprint of 2.5 mm x 3.0 mm, and an active area of 4.2 mm² excluding the bonding pads and the JTE field region. This large area 4H-SiC BJT has an emitter mesa width of 14 μ m and the same BE-spacing of 6 μ m. It also shows a good DC current gain of 23.6 and blocks over 1130 V with a specific on-resistance of 11.2 m Ω .cm².

The experimental results obtained from the double base epi-layer 4H-SiC BJTs show a high current gain, although the emitter injection efficiency may be lower in comparison to BJTs with lower base doping. This high current gain is achieved because the double base epilayer creates a built-in electric field in the base region and eliminates the need for ion implantation and high-temperature activation annealing, both leading to reduced base and surface recombination. The advantage of eliminating ion implantation lies not only in the elimination of implantation-induced crystal damages but also in the substantially simplified BJT fabrication process because many fabrication steps are eliminated,

including the critical steps of photolithography for creating ion implantation mask, shipping out samples for ion implantation, and high-temperature activation annealing. Work is on-going to design further improved BJT structure with a graded base doping that can be epitaxially grown continuously with the n+ emitter cap to maximize the built-in electric field in the base region and the BJT gain.

IV. SUMMARY

The first high voltage 4H-SiC BJT with double base epi-layers which are free of ion implantations and high temperature activation annealing have been successfully demonstrated. Because of the built-in electric field in the base and the elimination of implantation-induced damage and high-temperature annealing-induced surface roughness, a high current gain of 31.2 has been achieved for a BJT with an open base blocking voltage over 1.3 kV. Optimized design with gradually graded base doping and continuously grown base-emitter junction, once developed, can be expected to further improve the current gain and substantially simplify the BJT fabrication by elimination many time consuming fabrication steps.

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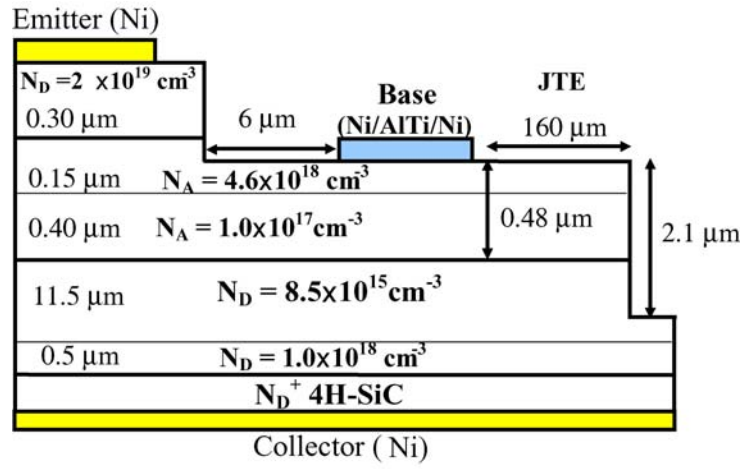


Fig. 1

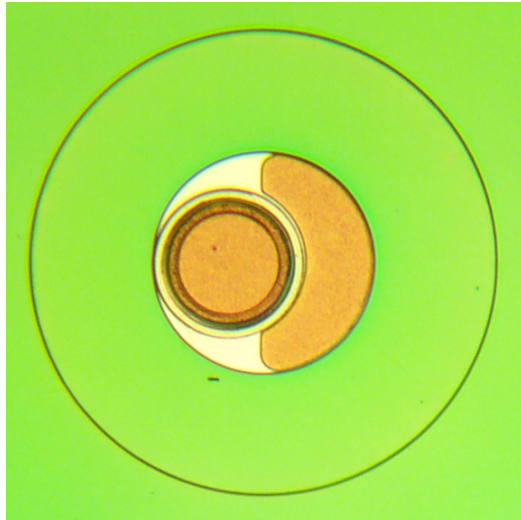


Fig. 2

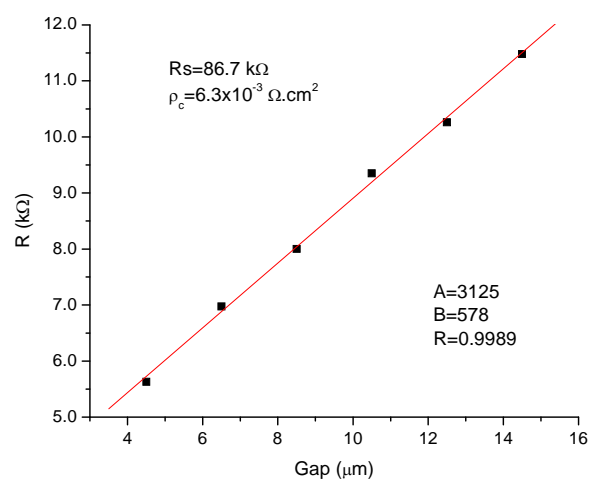


Fig. 3

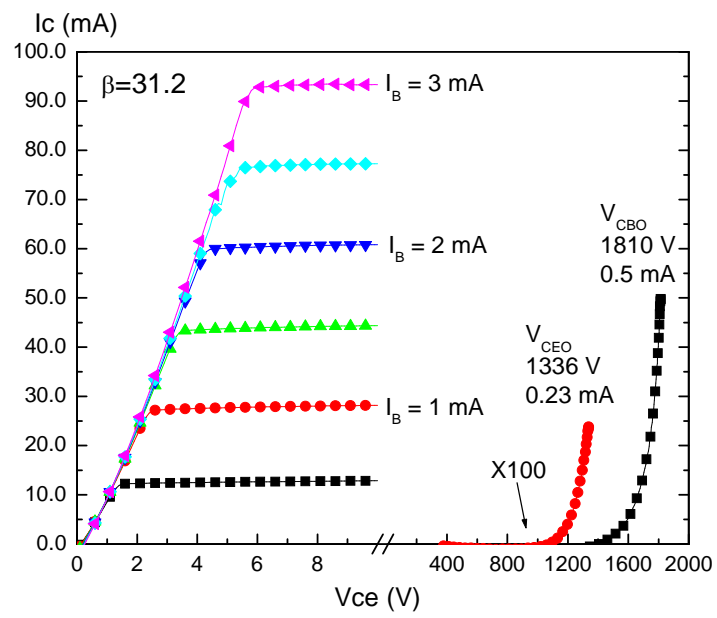


Fig. 4

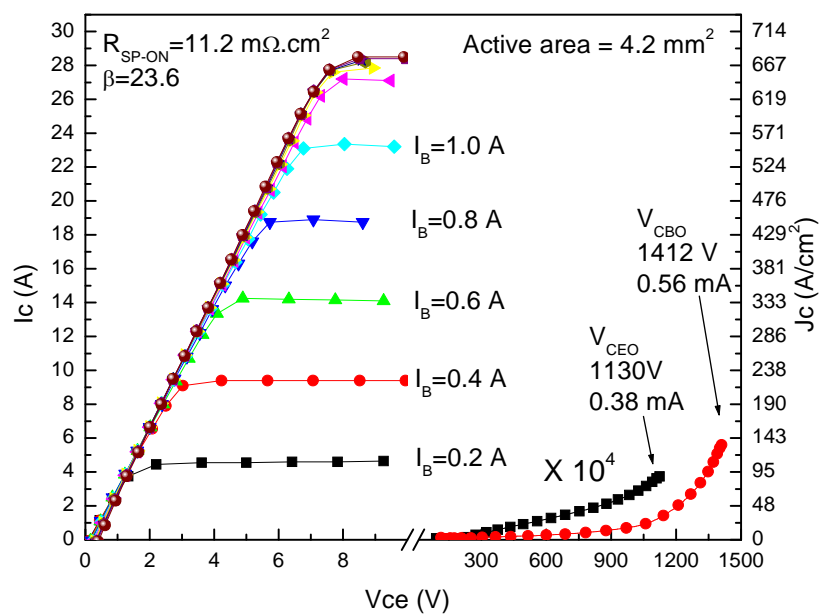


Fig. 5

FIGURE CAPTIONS

Fig. 1. Cross sectional view of the 4H-SiC BJT device

Fig. 2. Top view photo of a fabricated small area 4H-SiC BJT.

Fig. 3. TLM measurement results of the base Ohmic contact.

Fig. 4. I-V characteristics of a small area 4H-SiC BJT.

Fig. 5. I-V characteristics of a large area 4H-SiC BJT.

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